First, the Office Action indicates that the drawings do not show the rubbing direction of the lower substrate that is aligned parallel to the direction of the noise field created (1) between the **data bus line** and the counter or pixel electrodes and (2) between the **gate bus line** and the counter or pixel electrodes.

As to the noise field direction between the **data bus line** and the counter or pixel electrode, Fig. 3B, element B shows the rubbing direction B that is in parallel with the noise field 10 (shown in Figs. 3A and 3B). To clarify this, the second paragraph on page 10 (page 10, line 12 to page 11, line 1) has been amended.

The noise field direction between the **gate bus line** and the counter or pixel electrode is generally **perpendicular** to the noise field direction between the data bus line and the counter or pixel electrode. Fig. 3A shows that the noise field direction 10 runs between the data bus line 4 and the counter or pixel electrode, 6' or 8', and that the gate bus line 2 is perpendicular to the data bus line 4. This structure then leads to an understanding that the noise field direction running between the gate bus line 2 and the counter or pixel electrode, 6' or 8' is perpendicular to the noise field direction 10.

This formation of the noise fields is inherent to the present invention due to the structural layout of the bus lines and the pixel or counter electrode as discussed above and as shown by the drawings, in particular 3A and 3B. Therefore, Fig. 3A has been amended to accurately provide all labels in the drawings of all the noise field directions that are inherent to the present invention due to the structure as discussed above. Fig. 3A has been amended to add a reference numeral 11 to point out the noise filed direction between the gate bus line and the pixel or counter electrode which is generally perpendicular to the noise field direction 10.

It is respectfully submitted that no new matter has been added as the amendments made here is considered to be allowable by MPEP §2163.07(a), which states as follows:

> By disclosing in a patent application a device that **inherently** performs a function or **has a property**, operates according to a theory or has an advantage, a patent application necessarily discloses that function, theory or advantage, **even though it says nothing explicit concerning it. The application may later be amended to recite the function, theory or advantage without introducing prohibited new matter.** *In re Reynolds*, 443 F.2d 384, 170 USPQ 94 (CCPA 1971); *In re Smythe*, 480 F. 2d 1376, 178 USPQ 279 (CCPA 1973).

For further clarification of the presently claimed invention, these two noise field directions 10, 11 have been recited in n two separate claims. That is, Claim 13 has been added to recite the noise field 11 formed between the gate bus line and the counter or pixel electrode, and Claim 1 has been amended to recite the noise field 10 formed between the data bus line and the counter or pixel electrode.

Second, the Office Action indicates that the drawings do not show the counter electrode having a shape of a "box" and the pixel electrode having a shape of a "clamp."

The "box" shaped counter electrode 8' (as shown in Fig. 3A and 4) means that the counter electrode 8' has a "rectangular plate shape." As to the "clamp" shape (as described in the Specification and recited in Claim 2) means a "V" shape of a "clamp" (i.e., a claim generally has two legs with one end of each leg pinned together for pivoting purposes, thereby forming a "V" shape). Therefore, Fig. 3A has been amended to remove some extraneous lines that may not contribute to clear depiction of the shapes of the counter and pixel electrodes. The amended Fig. 3A more clearly shows the rectangular plate shape of the counter electrode 8' and the V shape of the pixel electrode 6'.

Third, the Office Action indicates that drawings do not show the distance between the counter electrodes because only one counter electrode is shown in the drawings. In response, Claim 6 has been amended to recite that --the distance [is] between the counter electrode in one pixel and another counter electrode in an adjacent pixel--.

For the reasons above, withdrawal of the objections to the drawings and the approval of the corrections of Figs. 3A and 3B are respectfully requested.

Claims

Claims 1-12 are currently pending before the present amendment. By the present amendment, Claims 1-9 have been amended and Claims 13-14 have been added. No new matter has been added.

Under 35 U.S.C. §112

Claims 1-12 stand rejected under 35 U.S.C. §112, ¶2, as being indefinite for failing to particularly point out and distinctively claim the subject matter, which Applicants regard as the invention.

As to Claim 1, the limitation regarding the noise field between gate bus line and the pixel and or counter electrode is deleted. For the same reason, the element "gate bus line" is also deleted in Claim 1. Thus, Claim 1 now recites, inter alia, a data bus line that is formed on the insulating layer (supported in Fig. 6), and the noise field between the data bus line and the pixel or counter electrode (supported in Fig. 3A).

The noise field formed between the gate electrode and the pixel or counter electrode is

now recited in Claim 13. Claim 13 also recites the gate bus line that is formed perpendicular to the data bus line (supported in Fig. 3A). As such, it is readily understood that a noise field formed between the counter or pixel electrode and the gate bus line that is oriented perpendicular to the data bus line.

As to Claims 2-3, the "patterned to have a shape of a clamp" refers to the "V" shaped pixel electrode 6' (Fig. 3A) as a "clamp" typically has two legs with one end of each leg being pinned together in the shape of V for pivoting purposes. To clarify this meaning, Claims 2-3 and the relevant paragraphs in the Specification have been amended.

As to Claim 6, this distance limitation found in Claim 6 has been amended for better clarification that the distance refers to the "distance between the counter electrode in one pixel and another counter electrode in an adjacent pixel."

Under 35 U.S.C. §102

Claims 1, 5, and 10-12 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,088,078 (Kim 078). The "et al." suffix appearing after a reference name is omitted.

As discussed above, Claim 1 has been amended and Claim 13 has been added such that the amended Claim 1 recites the noise field direction running between the data bus line and the counter or pixel electrodes, and the new Claim 13 recites the noise field direction running between the gate bus line and the counter or pixel electrodes.

As to Claim 1, to further distinguish from Kim 078, Claim 1 has been amended to incorporate the limitation of Claim 2 that the counter electrode has the "rectangular plate shape"

and the pixel electrode is V shaped.

One of the main differences between Kim 078 and the presently claimed invention is in the shapes of the counter and pixel electrodes and the arrangement of these electrodes in ways to create electric field patterns suitable for fringe field switching (FFS) mode. According to Kim 078, the counter electrode 24 is shaped as a non-plate, square frame having four sides, and the pixel electrode 25 is cross-shaped. However, the counter electrode recited in Claim 2 (and shown in Fig. 3A) is plate shape and rectangular (i.e., "box shaped"), and the pixel electrode recited in Claim 2 (and in accordance with Fig. 3A) is a plurality of V shaped electrodes, each of the two ends of each electrode is connected to an elongated electrical electrode.

The independent Claim 1, now amended, includes the limitation that the pixel electrode is made up of a plurality of "V" shaped conductive metals. The support for the "V" shaped electrode is well depicted in Fig. 3A and described in the Specification that the "V" shaped pixel electrode resembles a shape of a "clamp," which typically has two legs with one end of each leg pinned together for pivot and thus resembling the shape of the letter "V". Kim 078 does not disclose (or teach or suggest) the claimed "V" shaped pixel electrode.

Claim 13 is distinguished from Kim 078 since Kim 078 does not show the planar counter electrode; a plurality of V shaped pixel electrodes; and further the rubbing direction r1 of Kim 078 would be perpendicular to the noise field formed between the **gate bus line** and the counter or pixel electrode.

Claims 1, 3, and 9 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,745,207 (Asada).

Asada does not show the claimed "**rectangular plate shaped**" counter electrode as claimed in Claims 1 and 13.

Further, the presently claimed invention has the rubbing direction that is aligned with the direction of the noise field developed (1) between the data bus line and pixel or counter electrodes as in Claim 1 or (2) between the gate bus line and pixel or counter electrode as in Claim 13. Asada, however, does not show rubbing direction recited in Claim 1. As seen in Fig. 2-4 and 6, every embodiment of Asada shows the same alignment position of the liquid crystal molecules 6a that is lined up perpendicular to the noise field that may be present between a data bus line and the counter or pixel electrode. This shows that the rubbing direction of the liquid crystal molecules 6a are not in the direction of the noise field formed between the signal wiring 3 and the pixel or common electrodes 2,4 of Asada.

As a final note, Asada appears to be directed only to the IPS mode. That is, Asada is about creating **horizontal** electrical field in the liquid crystal layer, and, in order to achieve this, the pixel and common electrodes are all laid on the **same planar surface** (i.e., as shown in Fig. 1 of Asada, the elements 1,2,3,4,5 are all laid on one substrate; see also Asada col. 5, lines 5-13).

Unlike the IPS mode described in Asada, the FFS mode of the present invention has much more complicated E field arrangement that allows better viewing angle while preventing color shifts. To create this fringe field, the claimed invention places the pixel and counter electrodes on different layers separated by an insulating layer. Asada fails to show this.

Claims 1, 2, 5, and 10-12 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,256,081 (Lee).

It is respectfully submitted that Lee is not a proper §102(e) prior art reference against the present application, because Lee and the present application share a common inventive entity (i.e., Seung Hee LEE) and are assigned to a common assignee. It is noted that Applicants have perfected their priority date (i.e., December 5, 2000) by filing a certified copy of the Korean Patent Application No. 2000-72718 on December 4, 2001. Therefore, Lee is not a patent by "another" in the meaning of §102(e).

Claims 1 and 8 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application Number 2001/0001568 (Hiroshi). Claims 4 and 6 stand rejected under 35 U.S.C. §103(a) as being anticipated over Kim 078 in view of U.S. Patent No. 6,198,464 (Ota).

As to Hiroshi, as was the case in Asada, Hiroshi fails to show, inter alia, the rectangular plate shaped counter electrode. Hiroshi instead shows a typical IPS mode arrangement where the "common electrode 49" is **not plate shaped**. Ota too shows a typical IPS mode arrangement where the common electrode is **not rectangular plate shaped**. Further, neither Ota nor Kim 078 shows the claimed V shaped pixel electrodes.

Allowable Subject Matter

Claim 7 stand allowable if it is rewritten to overcome the rejection(s) under 35 U.S.C. §112, ¶2, set forth in the outstanding Office Action and to include all limitations of the base claim and any intervening claims.

In response, Claim 7 has been amended to place the claim in condition to overcome all rejections under 35 U.S.C. §112, ¶2, and also to include all limitations of the base claim and any intervening claims. Thus, allowance of Claim 7 is respectfully requested.

For the reasons set forth above, Applicants respectfully submit that Claims 1-14, now pending in this application, are in condition for allowance. This amendment is considered to be responsive to all points raised in the Office Action. Accordingly, Applicants respectfully request reconsideration and withdrawal of the outstanding rejections and earnestly solicit an indication of allowable subject matter. Should the Examiner have any remaining questions or concerns, the Examiner is encouraged to contact the undersigned attorney by telephone to expeditiously resolve such concerns.

Respectfully submitted,

Dated: 5/5/03

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DOCKET: CU-2746 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application:	Hyang Yul KIM	]
		]
Serial No:	10/005,060	] GRP ART UNIT: 2815
		]
Filed:	December 4, 2001	] Ex.: Landau, Matthew C.
		]
For:	LIQUID CRYSTAL DISPLAY DEVICE	]

SPECIFICATION - MARKED-UP VERSION

(IN THE REVISED USPTO FORMAT)

In the second paragraph, on page 1 (lines 14-22):

A1

As well known, a conventional liquid crystal display device has generally employed a twisted nematic (TN) mode, which has a disadvantage of narrow view angle. In order to solve the problem, a fringe field switching (FFS) mode liquid crystal display device has been proposed. ~~And, an FFS mode liquid crystal display device has been improved to have a clamp structure in order to prevent color shift of view angles by single domain.~~

In the last paragraph, on page 2, line 21 to page 3, line 2:

A2

Referring to the FIGS. 1A-1C, in order to obtain maximum transmittance, negative liquid crystals are rubbed by .+-.12.degree. to a gate bus line 2 and positive liquid crystals by .+-.78.degree. to the gate bus line. Therefore, early liquid crystal molecules 3 are controlled to correspond with the rubbing direction A (as shown in FIG. 1B).

In the first paragraph, on page 3, lines 3-5:

A3

Here, a Noise Field 10 (as shown in FIGS. 1A-1B) is formed between a data bus line 4 and a pixel electrode 6 or between the data bus line 4 and a counter electrode 8.

In the second paragraph, on page 5 (lines 12-17):

A4

Preferably, the counter electrode may have a shape of box (i.e., generally a planar, rectangular shape) made of a first ITO and the pixel electrode may be formed by patterning a second ITO to have a shape of clamp (i.e., a clamp having two legs with one end of each leg pinned together for pivoting so as to resemble generally a "V" shape) in one sub-pixel or to alternatively have a slant line (/) shape and an inverse-slant line (\) shape by sub-pixels (i.e., each generally V shaped pixel electrode being in a sub-pixel), thereby having FFS mode.

In the first paragraph, on page 9 (lines 2-14):

A5

According to the present invention, the counter electrode 8', made of a first ITO having a shape of box (or in a rectangular plate shape), the gate bus line 2, the counter electrode bus line 7, the data bus line 4 and TFT are formed in the same method as that of the conventional liquid crystal display. However, a pattern is formed in ~~a~~ the shape of a clamp--more specifically, a plurality of parts form the pixel electrode for one pixel and each part substantially resembles the shape of "V" in one sub-pixel--or formed to alternatively have a slant line (/) shape and an inverse-slant line (\) shape by sub-pixels, using the pixel electrode 6' made of a second ITO, in order to solve a color shift problem by compensation structure of the refractivity of the liquid crystal molecule 3.

In the first paragraph, page 10 (lines 4-11):

Generally, the noise field 10 is formed between the data bus line 4 and the pixel electrode 6' or the counter electrode 8'. ~~and~~ Another noise field 11 is formed between the gate bus line 2 and the pixel electrode 6' or the counter electrode 8'. When the rubbing is parallel to the gate bus line 2, the rubbing direction corresponds with that of the noise field 10 formed between the data bus line 4 and the pixel electrode 6' or the counter electrode 8'.

A6

In the last paragraph, page 10, (page 10, line 12 to page 11, line 1):

And, when the rubbing is perpendicular to the gate bus line 2, the rubbing direction corresponds with that of the noise field ~~10~~ 11 formed between the gate bus line 2 and the pixel electrode 6' or the counter electrode 8'. As a result, when positive liquid crystals are employed, the major axis of the liquid crystal molecule 3 is arranged to the rubbing direction and the polarity of spontaneous polarization of the liquid crystal molecule 3, generated by the electric field, is formed at the terminal of major axis of the liquid crystal molecule 3. Therefore, when the rubbing direction corresponds with that of the noise field 10 (as shown in FIG. 3B, element B), the liquid crystal molecules 3 are not affected by the noise field 10.

A7

DOCKET: CU-2746 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application:	Hyang Yul KIM	]
		]
Serial No:	10/005,060	] GRP ART UNIT: 2815
		]
Filed:	December 4, 2001	] Ex.: Landau, Matthew C.
		]
For:	LIQUID CRYSTAL DISPLAY DEVICE	]

CLAIMS - MARKED-UP VERSION

(IN THE REVISED USPTO FORMAT)

1. (Currently Amended) A liquid crystal display device comprising:

a lower substrate having a lower inner surface and a lower outer surface, wherein the lower substrate is rubbed in a rubbing direction for alignment of liquid crystal molecules; ~~and~~

a lower polarizing plate formed on the lower outer surface;

an upper substrate ~~confronting each other~~ having an upper inner surface and an upper outer surface, wherein the lower inner surface and the upper inner surface face each other at a distance in a substantially parallel manner;

an upper polarizing plate formed on the upper outer surface;

a counter electrode formed on a portion of the lower ~~substrate~~ inner surface, wherein the counter electrode has a rectangular plate shape;

an insulating layer formed on the counter electrode and the lower inner surface;

a pixel electrode formed on ~~the counter electrode with an~~ a portion of the insulating layer ~~interposed~~ , wherein the pixel electrode is patterned as a plurality of V-shaped electrical conductors;

~~a lower polarizing plate and an upper polarizing plate attached on respective outer sides of the lower and the upper substrates;~~

~~a gate bus line; and~~

a data bus line formed on a portion of the insulating layer, wherein a ~~rubbing direction of the lower substrate corresponds with a direction of~~ noise field is formed between the data bus line and the pixel electrode ~~or~~ and between the data bus line and the counter electrode, ~~and between the gate bus line and the pixel electrode or the counter electrode~~ and further wherein the rubbing direction of the lower substrate substantially corresponds to the direction of the noise field; and

a gate bus line formed substantially perpendicular to the data bus line on a different layer.

2. (Currently Amended) The liquid crystal display device according to claim 1, wherein the counter electrode ~~has a shape of box made of a first ITO~~ and the pixel electrode ~~is~~ are made of a transparent electrical conductor including an indium tin oxide (ITO) ~~formed by patterning a second ITOs to have a shape of clamp in one sub-pixel, or to alternatively have a slant line (/) shape and an inverse slant line (\) shape by sub-pixels, thereby having~~ for forming a fringe field switching (FFS) mode.

3. (Currently Amended) The liquid crystal display device according to claim 1, wherein the counter electrode and the pixel electrode are made of an opaque electrical conductor ~~metal and the counter electrode and the pixel electrode are respectively patterned to have a shape of clamp in one sub-pixel, or to alternatively have a slant line (/) shape and an inverse slant line (\) shape by sub-pixels thereby having~~ for forming an in plane switching (IPS) mode.

4. (Currently Amended) The liquid crystal display device according to claim 1, ~~wherein~~ further comprising a black matrix formed on the upper inner surface substantially covering the data bus line, wherein the rubbing direction of the lower substrate is substantially parallel to the gate bus line, ~~and~~ which is also substantially parallel to the direction of the noise field ~~is~~ formed between the data bus line and the counter electrode or between the data bus line and the pixel electrode ~~and therefore, black matrix of the upper substrate is narrowly formed on the data bus line~~.

5. (Currently Amended) The liquid crystal display device according to claim ~~1~~ 4, wherein the rubbing direction of the lower substrate is substantially parallel to the gate bus line and there is no black matrix formed on the upper inner surface of the upper substrate.

6. (Currently Amended) The liquid crystal display device according to claim 4, wherein the black matrix ~~of the upper substrate~~ formed on the upper inner surface has a width ~~the same as~~ that is substantially equal to or smaller ~~that~~ than the distance between the ~~counter electrodes~~ counter electrode in one pixel and another counter electrode in an adjacent pixel ~~, formed~~ with the data bus line ~~interposed~~ formed between the two counter electrodes of the two adjacent pixels.

7. (Currently Amended) ~~The~~ A liquid crystal display device ~~according to claim 6,~~ comprising:

a lower substrate having a lower inner surface and a lower outer surface, wherein the lower substrate is rubbed in a rubbing direction for alignment of liquid crystal molecules;

a lower polarizing plate formed on the lower outer surface;

an upper substrate having an upper inner surface and an upper outer surface, wherein the lower inner surface and the upper inner surface face each other at a distance in a substantially parallel manner;

an upper polarizing plate formed on the upper outer surface;

a counter electrode formed on a portion of the lower inner surface, wherein the counter electrode has a rectangular plate shape;

an insulating layer formed on the counter electrode and the lower inner surface;

a pixel electrode formed on a portion of the insulating layer;

a data bus line formed on a portion of the insulating layer, wherein a noise field is formed between the data bus line and the pixel electrode and between the data bus line and the counter electrode and further wherein the rubbing direction of the lower substrate substantially corresponds to the direction of the noise field;

Contd A8

a gate bus line formed substantially perpendicular to the data bus line; and

a black matrix formed on the upper inner surface substantially covering the data bus line,

wherein the rubbing direction of the lower substrate is substantially parallel to the gate bus line, which is also substantially parallel to the direction of the noise field formed between the data bus line and the counter electrode or between the data bus line and the pixel electrode, and

further wherein the black matrix ~~of the upper substrate~~ formed on the upper inner surface has a width of less than 6 μm that is substantially equal to or smaller than the distance between the counter electrode in one pixel and another

counter electrode in an adjacent pixel with the data bus line formed between the two counter electrodes of the two adjacent pixels.

8. (Currently Amended) The liquid crystal display device according to claim 13, wherein the rubbing direction of the lower substrate is perpendicular to the gate bus line, and the noise field is formed between the gate bus line and the counter electrode or between the gate bus line and the pixel electrode and therefore, black matrix of the upper substrate is formed on the gate bus line to have a width the same as or smaller than that of the gate bus line.

9. (Currently Amended) The liquid crystal display device according to claim ~~1~~ 8, wherein the rubbing direction of the lower substrate is perpendicular to the gate bus line and there is no black of the upper substrate.

10. (Original) The liquid crystal display device according to claim 1, wherein the upper substrate has a rubbing direction anti-parallel or parallel to that of the lower substrate.

11. (Original) The liquid crystal display device according to claim 1, wherein the lower polarizing plate has a polarizer axis corresponding with the rubbing direction of the lower substrate.

12. (Original) The liquid crystal display device according to claim 1, wherein the upper polarizing plate has an analyzer axis perpendicular to the rubbing direction of the lower substrate.

13. (New) A liquid crystal display device comprising:

a lower substrate having a lower inner surface and a lower outer surface, wherein the lower substrate is rubbed for alignment of liquid crystal molecules;

a lower polarizing plate formed on the lower outer surface;

an upper substrate having an upper inner surface and an upper outer surface,

wherein the lower inner surface and the upper inner surface face each other at a distance in a substantially parallel manner;

an upper polarizing plate formed on the upper outer surface;

a counter electrode formed on a portion of the lower inner surface;

an insulating layer formed on the counter electrode and the lower inner surface;

a pixel electrode formed on a portion of the insulating layer;

a data bus line formed on a portion of the insulating layer; and

a gate bus line formed substantially perpendicular to the data bus line, wherein a noise field is formed between the gate bus line and the pixel electrode and between the gate bus line and the counter electrode, and further wherein the rubbing direction of the lower substrate substantially corresponds to the direction of the noise field.

14. (New) The liquid crystal device of claim 13 further comprising a black matrix formed on the upper inner surface substantially covering the data bus line,

wherein the rubbing direction of the lower substrate is substantially parallel to the gate bus line, which is also substantially parallel to the direction of the noise field formed between the data bus line and the counter electrode or between the data bus line and the pixel electrode, and

further wherein the black matrix formed on the upper inner surface has a width of less than 6 μm that is substantially equal to or smaller than the distance between the counter electrode in one pixel and another counter electrode in an adjacent pixel with the data bus line formed between the two counter electrodes of the two adjacent pixels.